Polar codes are a trending family of forward error correction codes currently gaining a place in the realm of digital communications, which exhibit a particularly high performance while requiring a low-complexity implementation. They were first adopted by the 3GPP 5G NR standard.

Rate-Flexible Polar Encoder

The Creonic Polar Encoder IP core is a scalable solution featuring code-rate flexibility, high throughput and very low latency on state-of-the-art FPGAs. Since a polar encoder normally requires information data to be presented in a certain way at its input, the Creonic Polar Encoder IP takes care of this in a pre-encoding stage. This important feature, with aid of AXI4-Stream interface ports, allows a very straight-forward integration of the core into any system.

Benefits

- Easy design-time parameterization of block length and supported code rates, for adjustment of resource utilization
- On-the-fly configuration of the code-rate on a block-by-block basis
- Does not require an extra IP to prepare the input data for encoding
- High code-rate granularity
- AXI4-Stream for easy integration
- Available for ASIC and FPGAs (AMD Xilinx, Intel, Microchip)

Performance Figures

- Maximum latency $T_{latency} < 40ns$ at 500 MHz
- Maximum coded throughput:
  - 77 Gbit/s (128 bits at 600 MHz)
  - 153 Gbit/s (256 bits at 600 MHz)
  - 281 Gbit/s (512 bits at 550 MHz)
  - 512 Gbit/s (1024 bits at 500 MHz)

Features

- Fully-pipelined architecture
- Support for systematic and non-systematic encoding
- Support for coded block lengths of up to 1024 bits
- Support for a wide variety of code-rates (1/8, 1/4, 3/8, 1/2, 5/8, 3/4, 13/16, 7/8)

Applications

- Satellite communication
- Wireless communication
- Applications with highest demands on forward error correction
- Applications with the need for a wide range of code rates

Deliverables

- VHDL source code or netlist
- HDL simulation models, e.g. for Aldec's RivieraPRO
- VHDL testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation

Rate-Flexible Polar Decoder

The Creonic Successive-Cancellation Polar Decoder IP core is a scalable solution featuring code-rate flexibility, high throughput and very low latency on state-of-the-art FPGAs. Its unique pipeline architecture can be customized at design-time to meet the desired specifications and deliver best performance on any target technology. In addition, the core features AXI4-Stream interface ports, which make it easy to use, and allow a very straightforward integration into any system.

Benefits

- Easy design-time parameterization of block length, soft-value quantization, and supported code rates, for adjustment of resource utilization.
- On-the-fly configuration of the code rate on a block-by-block basis
- High code-rate granularity.
- AXI4-Stream for easy integration
- Available for ASIC and FPGAs (AMD Xilinx, Intel, Microchip).

Performance Figures

- Coded throughput of $\approx$ 195 Gbit/s with a coded block length of 1024 bits at 190 MHz.
- BER 10^{-6} with QPSK and code rate 1/2 at
  - E_B/N_0 = 5.8 dB (128 bits)
  - E_B/N_0 = 5.3 dB (256 bits)
  - E_B/N_0 = 4.9 dB (512 bits)
  - E_B/N_0 = 4.1 dB (1024 bits)

Features

- Fully-pipelined architecture
- Compliant with 3GPP construction of Polar Codes
- Support for coded block lengths of up to 1024 bits
- Support for a wide variety of code-rates (1/8, 1/4, 3/8, 1/2, 5/8, 3/4, 13/16, 7/8)

Applications

- Satellite communications
- Mobile communications
- Applications with the highest demands on forward error correction
- Applications with the need for a wide range of code rates

Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models, e.g. for Aldec's RivieraPRO
- VHDL testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation

About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

Contact

Creonic GmbH	Phone:	+49 631 3435 9880	Twitter:	Creonic_IPCores
Bahnhofstr. 26-28	Fax:	+49 631 3435 9889	Facebook:	Creonic
67655 Kaiserslautern	Web:	www.creonic.com	LinkedIn:	Creonic
Germany	E-mail:	sales@creonic.com		